IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/632,155	Filing Date:	July 30, 2003
Confirmation No.:	1880		
First Named Inventor:	Yi Ding		
Assignee:	ProMOS Technologies Inc.		
Examiner:	Nhu, David	Art Unit:	2818
Attorney Docket No.:	M-15222 US		

San Jose, California
May 2, 2006

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST TO RETURN INITIALED FORMS PTO-1449S

Dear Sir:

Enclosed are copies of forms PTO-1449s (4 pages) submitted with Information Disclosure Statements filed July 30, 2003 and September 17, 2003. Applicant has not received copies of the forms initialed by the Examiner. Applicants request the form to be initialed by the Examiner and returned to the undersigned.

EXPRESS MAIL LABEL NO.:

EV 861 968 608 US

Respectfully submitted,

Michael Shenker

Michael Shenker
Attorney for Applicant(s)
Reg. No. 34,250

Law Offices of
MacPherson Kwok Chen Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
Tel: (408) 392-9250
Fax: (408) 392-9262

U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-15222 US	Unassigned
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Yi Ding	
	Filing Date	Group
	Filed Herewith	Unassigned

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,402,371	28 Mar. 1995	Ono			
	AB	5,856,943	5 Jan. 1999	Jenq			
	AC	6,057,575	2 May 2000	Jenq			
	AD	6,130,129	10 Oct. 2000	Chen			
	AE	6,134,144	17 Oct. 2000	Lin et al.			
	AF	6,171,909	9 Jan. 2001	Ding et al.			
	AG	6,200,856	13 Mar. 2001	Chen			
	AH	6,261,903	17 Jul. 2001	Chang et al.			
	AI	6,326,661	4 Dec. 2001	Dormans et al.			
	AJ	6,355,524	12 Mar. 2002	Tuan et al.			
	AK	6,365,457	2 Apr. 2002	Choi			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AL	Shirota, Riichiro "A Review of 256Mbit NAND Flash Memories and NAND Flash Future Trend," February 2000, Nonvolatile Memory Workshop in Monterey, California, pages 22-31.
	AM	Naruke, K.; Yamada, S.; Obi, E.; Taguchi, S.; and Wada, M. "A New Flash-Erase EEPROM Cell with A Sidewall Select-Gate On Its Source Side," 1989 IEEE, pages 604-606.
	AN	Wu, A.T.; Chan T.Y.; Ko, P.K.; and Hu, C. "A Novel High-Speed, 5-Volt Programming EPROM Structure With Source-Side Injection," 1986 IEEE, 584-587.
	AO	Mizutani, Yoshihisa; and Makita, Koji "A New EPROM Cell With A Sidewall Floating Gate Fro High-Density and High Performance Device," 1985 IEEE, 635-638.
	AP	Ma, Y.; Pang, C.S.; Pathak, J.; Tsao, S.C.; Chang, C.F.; Yamauchi, Y.; Yoshimi, M. "A Novel High Density Contactless Flash Memory Array Using Split-Gate Source-Side-Injection Cell for 5V-Only Applications," 1994 Symposium on VLSI Technology Digest of Technical Papers, pages 49-50.
	AQ	Mih, Rebecca et al. "0.18um Modular Triple Self-Aligned Embedded Split-Gate Flash Memory," 2000 Symposium on VLSI Technology Digest of Technical Papers, pages 120-121.
	AR	Ma, Yale et al., "A Dual-Bit Split-Gate EEPROM (DSG) Cell in Contactless Array for Single Vcc High Density Flash Memories," 1994 IEEE, 3.5.1-3.5.4.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-15222 US	Unassigned
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Yi Ding	
	Filing Date	Group
	Filed Herewith	Unassigned

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AS	6,437,360	20 Aug. 2002	Cho et al.			
	AT	6,438,036	20 Aug. 2002	Seki et al.			
	AU	6,486,023	26 Nov. 2002	Nagata			
	AV	6,541,324	1 Apr. 2003	Wang			
	AW	2002/0064071 A1	30 May 2002	Takahashi et al.			
	AX	2002/0197888 A1	26 Dec. 2002	Huang et al.			
	AY	6,266,278	24 Jul. 2001	Harari et al.			
	AZ	5,901,084	4 May 1999	Ohnakado			
	BA	6,518,618	11 Feb. 2003	Fazio et al.			
	BB	6,541,829	1 Apr. 2003	Nishinohara et al.			
	BC	6,414,872	2 Jul. 2002	Bergemont et al.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	BD	Spinelli, Alessandro S., "Quantum-Mechanical 2D Simulation of Surface-and Buried-Channel p-MOS,"2000 International Conference on Simulation of Semiconductor Processes and Devices: SISPAD 2000, Seattle, WA September 6-8, 2000
	BE	Kim, K.S. et al. "A Novel Dual String NOR (DuSnor) Memory Cell Technolgy Scalabe to the 256 Mbit and 1 Gbit Flash Memories," 1995 IEEE 11.1.1-11.1.4
	BF	Bergemont, A. et al."NOR Virtual Ground (NVG)- A New Scaling Concept for Very High Density FLAS EEPROM and its Implementation in a 0.5 um Process," 1993 IEEE 2.2.1-2.2.4
	BG	Van Duuren, Michiel et al., "Compact poly-CMP Embedded Flash Memory Cells For One or Two Bit Storage," Philips Research Leuven, Kapeldreef 75, B3001 Leuven, Belgium, pages 73-74.
	BH	
	BI	
	BJ	

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-15222 US	10/632,155
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant	
(Use several sheets if necessary)	Yi Ding	
	Filing Date	Group
	July 30, 2003	Unassigned

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
	AO						
	AP						
	AQ						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	United States Patent Application No. 10/440,466, entitled "Fabrication Of Conductive Gates For Nonvolatile Memories From Layers With Protruding Portions," Filed on May 16, 2003; Attorney Docket No.: M-12979 US.
	AS	United States Patent Application No. 10/440,005, entitled "Fabrication of Dielectric On A Gate Surface To Insulate The Gate From Another Element Of An Integrated Circuit," Filed on May 16, 2003; Attorney Docket No.: M-15203 US.
	AT	United States Patent Application No. 10/440,508, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories Having Select, Floating And Control Gates," Filed on May 16, 2003; Attorney Docket No.: M-15204 US.
	AU	United States Patent Application No. 10/440,500, entitled "Integrated Circuits With Openings that Allow Electrical Contact To Conductive Features Having Self-Aligned Edges," Filed on May 16, 2003; Attorney Docket No.: M-15205 US.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-15222 US	10/632,155
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant	
(Use several sheets if necessary)	Yi Ding	
	Filing Date	Group
	July 30, 2003	Unassigned

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AV	United States Patent Application No. 10/393,212, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on March 19, 2003; Attorney Docket No.: M-12902 US.
	AW	United States Patent Application No. 10/411,813, entitled "Nonvolatile Memories With A Floating Gate Having An Upward Protrusion," Filed on April 10, 2003; Attorney Docket No.: M-12903 US.
	AX	United States Patent Application No. 10/393,202, entitled "Fabrication of Integrated Circuit Elements In Structures With Protruding Features," Filed on March 19, 2003; Attorney Docket No.: M-15151 US.
	AY	United States Patent Application No. 10/631,941, entitled "Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate," Filed on July 30, 2003; Attorney Docket No.: M-15171 US.
	AZ	United States Patent Application No. 10/632,007, entitled "Arrays Of Nonvolatile Memory Cells Wherin Each Cell Has Two Conductive Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15223 US.
	BA	United States Patent Application No. 10/631,452, entitled "Fabrication Of Dielectric For A Nonvolatile Memory Cell Having Multiple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15229 US.
	BB	United States Patent Application No. 10/632,154, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories In Which A Memory Cell Has Mutiple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15230 US.
	BC	United States Patent Application No. 10/631,552, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on July 30, 2003; Attorney Docket No.: M-12902-1P US.
	BD	United States Patent Application No. 10/632,186, entitled "Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate And Having Upward Protrusions," Filed on July 30, 2003; Attorney Docket No.: M-15241 US.
	BE	
	BF	
	BG	
	BH	

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.